**Amendments to the Specification:**

Please replace the paragraph at page 4, lines 3-5 with the following amended paragraph:

Page 4, lines 3-5

Referring to FIG. 1B, a plasma enhanced dry etching is implemented by utilizing the photoresist pattern 122 as an etching mask to form an oxide layer pattern 112 having a contact hole 125 wherein the aspect ratio is about ~~8-12~~ 8:1 to 12:1.

Please replace the paragraph at page 8, lines 8-11 with the following amended paragraph:

Page 8, lines 8-11

The contact hole is formed according to the above-described processes in a silicon oxide layer having a thickness in a range of about 20,000-40,000Å. A contact hole having an aspect ratio in a range of about ~~8-17~~ 8:1 to 17:1 and a diameter in a range of about 150-250 nm can thereby be advantageously formed.

Please replace the paragraph at page 13, lines 1-3 with the following amended paragraph:

Page 13, lines 1-3

Referring to FIG. 4B, a plasma enhanced dry etching procedure was implemented by utilizing the photoresist pattern 222 as an etching mask to form an oxide layer pattern 212 having a contact hole 225 having aspect ratio of about ~~8-12~~ 8:1 to 12:1.

Please replace Table 1 at page 18, between lines 10 and 13 with the following amended Table:

Page 18, Table 1

**Table 1**

| | FIG. 7A | FIG. 7B | FIG. 7C | FIG. 7D |
|---|---|---|---|---|
| Size (nm) | 432 | 369 | 277 | 202 |
| Depth (Å) | 34101 | 33731 | 32902 | 31675 |
| A/R | ~~7.9~~ 7.9:1 | ~~9.1~~ 9.1:1 | ~~11.9~~ 11.9:1 | ~~15.7~~ 15.7:1 |

Please replace the paragraph at page 19, lines 5-11 with the following amended paragraph:

Page 19, lines 5-11

From the results, it was confirmed that a contact hole having a diameter in a range of about 150-250 nm, a depth of about 20,000-40,000Å, an aspect ratio of about ~~8-17~~ 8:1 to 17:1 and a good profile was obtained by etching according to the present invention. As one kind of contact hole satisfying the above-described conditions, an MC (metal contact hole) for connecting a metal layer formed on a silicon oxide layer above a capacitor with an impurity doped region formed on a substrate in a DRAM device may be mentioned.